## REMARKS

In response to the Office Action mailed on May 11, 2004, Applicant wishes to enter the following remarks for the Examiner's consideration. Claims 1-9, 11-15 are rejected. Claim 10 is allowed. Claims 1-15 are pending in the application.

Applicant has amended claims 5, 6 and 15 in response to the Examiner's 35 USC 112, second paragraph, rejection of claims 5-9, 12-13, and 15. Claims 5 and 6 have been amended to remove the reference to the fifth and sixth transistors as comprising a current mirror. Moreover, Applicant has amended claims 5 and 6 to correct grammatical errors not related to issues of patentability and not in response to the 35 USC 112, second paragraph, rejection of claim 5 and claim 6. No new matter has been added. Claim 15 has been amended to replace "the negative input terminal" with the "the negative terminal". As noted by the Examiner, the changes to claims 5, 6 and 15 are supported by claims and specification and no new matter requiring further search has been introduced. In light of this change, Applicant respectfully requests reconsideration and allowance of claims 5-9, 12-13 and 15 at the Examiner's earliest convenience.

The Examiner has rejected claims 1-4, 11, and 14 under 35 USC 102(b) as being anticipated by Nishioka et al (hereinafter referred to as Nishioka). Applicant respectfully traverses this rejection of the claims.

Applicant respectfully submits that the 102(b) rejection of these claims is defective and should be withdrawn. MPEP 2131 provides that a claim is anticipated only if each and every element of a claim is found in a single prior art reference. Contrary to the examiner's assertion that all elements are disclosed in Nishioka, not all the elements are as will be described. The rejection is thus unsupported by the art and should be withdrawn.

With regard to claim 1, Applicant notes that Nishioka discloses a voltage to current conversion circuit (Abstract, Title, and Fig. 3), while Applicant's claim 1 is directed to a current amplifier cell. Nishioka does not teach, disclose, suggest or otherwise

anticipate a current amplifier circuit. And FIG. 3 of Nishioka which the Examiner refers to teaches a voltage to current conversion circuit not a current amplification circuit. In fact, Nishioka teaches away from the Applicant's claim 1, since Nishioka teaches a voltage input and a current output (col 1 lines 40-45, col 2, lines 1-5, and col 2, lines 38-40) and does not teach, suggest, disclose or otherwise anticipate a input current signal which can then be amplified. And, significantly, Examiner has not pointed out with particularity where such teaching occurs. In addition to the teaching that Nishioka does not disclose a voltage to current conversion circuit, Nishioka also does not teach, suggest, disclose or otherwise anticipate the use of two output signals. And, significantly, Examiner has not shown with particularity where such teaching occurs. Applicant further notes that there is no teaching in Nishioka of using a second output signal in a feedback application, because there is not a second output signal taught, anticipated or suggested in Nishioka. Applicant submits that the rejection of claim 1 is improper in light of the above arguments and should be withdrawn. Furthermore, Applicant has amended claim 1 to give the preamble patentable weight. No new matter has been introduced and this amendment is not being done for purposes related to patentability as the claim as filed described a current amplifier cell, which the Nihshioka reference clearly does not do. Rather, the amendment only serves to better clarify the subject matter of the claimed invention for this claim. Reconsideration and allowance of claim 1 is requested at the Examiner's earliest convenience.

With regard to claim 2, Applicant notes that the interconnections of Q6, Q7 and current source 22 of Nishioka are not as claimed in Applicant's claim 2. Q6 and Q7 are not coupled at their control terminals as stated in Applicant's claim 2, and the control terminal of Q7 does not receive an input signal. Furthermore, only the second terminal of Q7 is coupled to the Examiner's asserted Q8-Q9 gain stage. Thus, FIG. 3 of Nishioka does not teach, suggest or anticipate the elements of claim 2, and therefore Applicant submits that the rejection of claim 2 is improper in light of the above arguments and should be withdrawn. Reconsideration and allowance of claim 2 is requested at the Examiner's earliest convenience.

Claims 2-4, and 11 depend from claim 1 and although additional arguments could be made for the patentability of each of the claims, such arguments are believed

unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action. Reconsideration and allowance of claims 2-4, and 11 are requested at the Examiner's earliest convenience.

With regard to claim 14, Applicant strenuously objects to the Examiner's assertion that FIG. 3 of the Nishioka reference teaches, suggests or otherwise anticipates Applicant's claim 14. There is no teaching, suggestion or anticipation of a current amplifier cell in Nishioka. And, significantly, Examiner has not noted with particularity where such teaching occurs in the Nishioka reference. Therefore, since not all elements of claim 14 are taught, suggested or anticipated by Nishioka, Applicant asserts that the Examiner rejection of claim 14 is improper. Moreover, Applicant has amended claim 14 to correct grammatical errors not related to issues of patentability and not in response to the rejection of this claim over Nishioka. No new matter has been added. Reconsideration and allowance of claim 14 is hereby requested at the examiner's earliest convenience.

Applicant notes that claim 10 is allowed. In light of the foregoing, a Notice of Allowability of all pending claims 1-15 is now respectfully requested.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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